IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. **RA043D2C3C2**)

In the Application of:	)
	)
FARMWALD ET AL.	)
	)
Serial No: Continuation of 09/492,982	)
	)
Filed: Herewith	)
	)
Title: MEMORY DEVICE HAVING A VARIABLE DATA OUTPUT LENGTH (As Amended)	)

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application, kindly amend the application as follows:

IN THE ABSTRACT:

Please delete the Abstract of the Disclosure and substitute the attached Abstract of the Disclosure.

IN THE TITLE:

Please delete the title and substitute --MEMORY DEVICE HAVING A VARIABLE DATA OUTPUT LENGTH--.

IN THE SPECIFICATION:

On page 1, line 8, insert --This application is a continuation of Application No. 09/492,982, filed January 27, 2000 (pending); which is a continuation of Application No. 09/252,997, filed February 19, 1999 (now U.S. Patent 6,034,918), which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (now U.S. Patent 6,038,195), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No. 08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).--

On page 3, line 9, delete "micro-processor" and substitute --microprocessor--.

On page 6, line 1, delete "4,646,279" and substitute --4,646,270--.

On page 10, line 18, delete "Figure 7 shows" and substitute --Figures 7a and 7b show--.

On page 10, line 21, delete "Figure 8 shows" and substitute --Figures 8a and 8b show--.

On page 11, line 14, insert:

--Figure 16 is a block diagram representation of a set of internal registers within each device illustrated in Figure 2.--

On page 14, line 3, replace "Each" with --With reference to Figure 16, each--.

On page 14, line 4, after "registers" insert --170--.

On page 14, line 5, after the **first** occurrence of "register" insert --171--.

On page 14, line 5, after the **second** occurrence of "register" insert --174--.

On page 14, line 6, after the **first** occurrence of "register" insert --175--.

On page 14, line 8, after "registers" insert --172--.

On page 14, line 10, after "registers" insert --173--.

On page 14, line 17, after "register" insert --171--.

On page 14, line 20, after the **first** occurrence of "registers" insert --173--.

On page 14, line 20, after the **second** occurrence of "registers" insert --175--.

On page 14, line 20, after the **third** occurrence of "registers" insert --172--.

On page 14, line 22, after "registers" insert --173--.

On page 21, line 15, after "registers" insert --173--.

On page 34, line 4, after "devices" insert --do--.

On page 35, line 25, after "registers" insert --170--.

On page 36, line 10, after "registers" insert --173--.

On page 36, line 15, after "register" insert --171--.

On page 36, line 12, after "registers" insert --172--.

On page 38, line 25, after "register" insert --173--.

On page 39, line 6, after "register" insert --173--.

On page 41, line 1, delete "or' "and substitute -- or--.

On page 45, line 17, delete "Fig. 7" and substitute --Figures 7a and 7b--.

On page 47, line 2, delete "Figure 8" and substitute --Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute --from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 58, line 22, after "clocks" insert --73 and 74, respectively--.

On page 60, line 10, after "147" insert --A, B-.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

--151. A method of operation of a synchronous memory device, wherein the memory device includes an array of memory cells, the method of operation of the memory device comprises:

receiving an external clock signal;

receiving block size information, wherein the block size information defines an amount of data to be output by the memory device in response to a read request;

receiving a first read request synchronously with respect to a rising edge transition of the external clock signal; and

outputting the amount of data, in response to the first read request, the amount of data corresponding to the block size information.

152. The method of claim 151 wherein the block size information defines an amount of data to be input by the memory device in response to a write request, the method further including:

receiving a first write request synchronously with respect to a transition of the external clock signal; and

inputting the amount of data, in response to the first write request, the amount of data corresponding to the block size information.

153. The method of claim 152 wherein a first portion of data is sampled, in response to the first write request, after a delay time transpires.

154. The method of claim 151 wherein the amount of data is output synchronously with respect to the external clock signal.

155. The method of claim 154 wherein a first portion of data is output synchronously with respect to a rising edge transition of the external clock signal and a second portion of data is output synchronously with respect to a falling edge transition of the external clock signal.

156. The method of claim 151 wherein the first read request is specified by an operation code.

157. The method of claim 156 wherein the operation code includes precharge information.

158. The method of claim 156 wherein the operation code is included in a request packet.

159. The method of claim 158 wherein the block size information and the operation code are both included in the same request packet.

160. The method of claim 158 wherein the request packet includes address information.

161. The method of claim 151 wherein the block size information is sampled synchronously with respect to the external clock signal.

162. The method of claim 151 further including:

receiving a code which is representative of a number of clock cycles of the external clock signal to transpire before the memory device responds to the first read request; and

storing the code in a register.

163. The method of claim 162 wherein the memory device outputs a first portion of data after the number of clock cycles of the external clock signal transpire.

164. The method of claim 151 wherein the block size information is a binary code.

165. A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells, the method of controlling the memory device comprises:

providing block size information to the memory device, synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request; and

issuing a first read request to the memory device, wherein the memory device receives the first read request synchronously with respect to a transition of the external clock signal.

166. The method of claim 165 further including receiving the amount of data from the memory device.

167. The method of claim 165 further including providing a code to the memory device, wherein the code is representative of a number of clock cycles of the external clock signal to transpire before the memory device responds to the first read request.

168. The method of claim 167 further including providing a set register request to the memory device, wherein the memory device stores the code in a register in response to the set register request.

169. The method of claim 165 wherein the first read request is specified by an operation code.

170. The method of claim 169 wherein the operation code includes precharge information.

171. The method of claim 169 wherein the operation code is included in a request packet.

172. The method of claim 171 wherein the block size information is included in a request packet.

173. The method of claim 171 wherein the block size information and the operation code are both included in the same request packet.

174. The method of claim 171 wherein the request packet further includes address information.

175. The method of claim 165 wherein the block size information is a binary code.

176. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to receive block size information synchronously with respect to the external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request; and

a plurality of output drivers to output the amount of data corresponding to the block size information, wherein the first amount of data is output in response to the read request.

177. The memory device of claim 176 wherein the amount of data is output synchronously with respect to the external clock signal.

178. The memory device of claim 177 wherein a first portion of data is output synchronously with respect to a rising edge transition of the external clock signal and a second portion of data is output synchronously with respect to a falling edge transition of the external clock signal.

179. The memory device of claim 176 wherein the first read request is specified by an operation code.

180. The memory device of claim 179 wherein the operation code is included in a request packet.

181. The memory device of claim 180 wherein the block size information is included in a request packet.

182. The memory device of claim 181 wherein the block size information and the operation code are included in the same request packet.

183. The memory device of claim 179 wherein the operation code includes precharge information.

184. The memory device of claim 176 further including a programmable register to store a value which is representative of a number of clock cycles of the external clock signal to transpire before the memory device responds to a read request.

185. The memory device of claim 176 wherein the block size information defines an amount of data to be input in response to a write request.

186. The memory device of claim 185 wherein the input receiver circuitry samples a first portion of the amount of data in response to the write request.

187. The memory device of claim 186 wherein the input receiver circuitry samples the first portion of the amount of data, in response to the write request, after a delay time transpires.

188. The memory device of claim 176 further including delay lock loop circuitry coupled to the clock receiver circuitry to generate an internal clock signal, wherein the plurality of output drivers output data in response to the internal clock signal.

189. The method of claim 176 wherein the first block size information is a binary code.--

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application No. 09/492,982 which is a continuation of Application No. 09/252,997 (now U.S. Patent 6,034,918). Application Serial No. 09/492,982 is pending.

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/492,982, filed January 27, 2000 (pending); which is a continuation of Application No. 09/252,997 (now U.S. Patent 6,034,918), which is a continuation of Application No. 09/196,199, filed on November 20, 1998 (now U.S. Patent 6,038,195), which is a continuation of Application No. 08/798,520, filed on February 10, 1997 (now U.S. Patent 5,841,580); which is a division of Application No.

08/448,657, filed May 24, 1995 (now U.S. Patent 5,638,334); which is a division of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation or related U.S. application data identified above. No new matter has been added.

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-189 to more fully protect the instant invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, Figures 2, 4, and 10-13; page 14, line 3 to page 16, line 7; page 20, line 14 to page 21, line 20; page 22, line 11 to page 25, line 8; page 27, line 1 to page 28, line 20; page 46, line 19 to page 48, line 17; page 53, line 23 to page 59, line 2; page 71, line 20 to page 72, line 21; page 73, lines 20 to page 74, line 31; and page 115, lines 10-22.

Applicants have also amended the specification to correct obvious spelling, typographical and grammatical errors. No new matter has been added.

In addition, a new Abstract of the Disclosure is attached hereto. No new matter has been added.

Finally, accompanying this Preliminary Amendment is a Request to Approve Drawing Changes. Applicants have amended the drawings to show every feature of the invention specified in the claims. To that end, Applicants submit herewith new Figure 16, and amended Figure 10. A copy of Applicants Request to Approve Drawing Changes is attached.

New Figure 16 is added to illustrate, among other things, access-time register(s) 173. Figure 16 illustrates one embodiment of the internal registers within each device illustrated in Figure 2. Support may be found in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Respectfully submitted,

Date: Feb. 7, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325

ABSTRACT OF THE DISCLOSURE

A synchronous memory device and methods of operation and controlling such a device. The method of controlling the memory device includes providing block size information to the memory device, synchronously with respect to an external clock signal, wherein the block size information defines an amount of data to be output by the memory device in response to a read request. The method further includes issuing a first read request to the memory device, wherein the memory device receives the first read request synchronously with respect to a transition of the external clock signal.

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Assistant Commissioner for Patents
Washington, DC 20231

REQUEST TO APPROVE DRAWING CHANGES

Dear Sir:

Attached hereto is new Figure 16. Figure 16 illustrates the internal registers which reside in each device illustrated in Figure 2. This embodiment is described in the specification at page 14, lines 3-21 and page 53 lines 4-21. No new matter has been added.

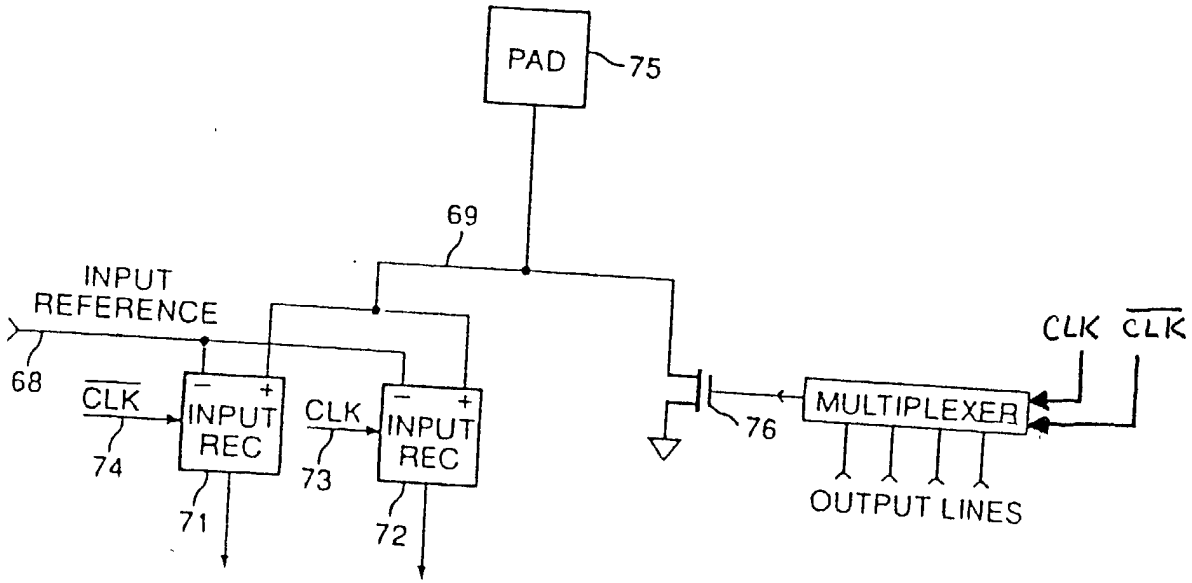
Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, specifically, page 55, line 12-16 and page 58, lines 13-23. Also attached, is a photocopy of Figure 10 with the proposed changes indicated in red. No new matter has been added.

Applicants respectfully request that the proposed new Figure 16 be approved by the Examiner. Applicants also respectfully request approval of the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached hereto.

Respectfully submitted,

Date: Feb 7, 2001

Neil A. Steinberg
Reg. No. 34,735
650-947-5325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CLK
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INPUT
REC
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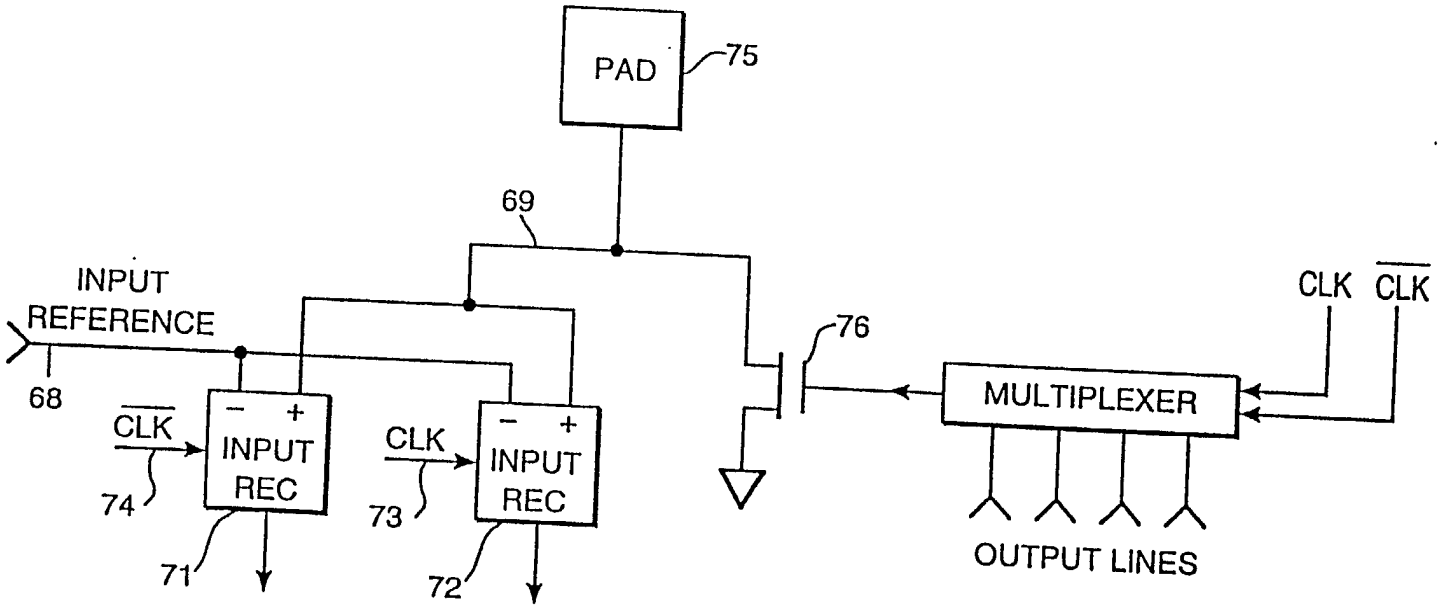
CLK
73
INPUT
REC
72
76
MULTIPLEXER
CLK
CLK
OUTPUT LINES

FIG. 10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REFERENCE
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CLK
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REC
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CLK
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INPUT
REC
72
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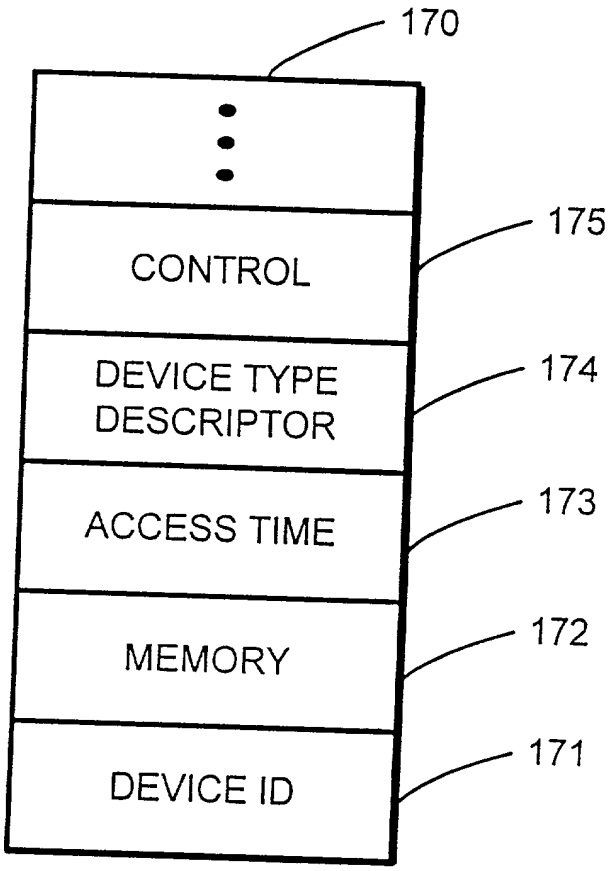
MULTIPLEXER
CLK
CLK
OUTPUT LINES

FIG_ 10


170
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ACCESS TIME
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MEMORY
172
DEVICE ID
171

FIG. 16